CLAIMS

What is claimed is:

1. An apparatus, comprising:

a first memory cell coupled to a first bit line;

a second memory cell coupled to a second bit line;

an address decoder coupled to the first and second memory cells to enable access to the first and second memory cells; and

a comparator circuit coupled to the first and second bit lines to compare the voltage level on the first bit line with the voltage level on the second bit at a time when data is output from the first memory cell on the first bit line and from the second memory cell on the second bit line.

2. The apparatus of claim 1, wherein the address decoder decodes part of a memory address.

3. The apparatus of claim 1, wherein the first and second memory cells are dynamic RAM memory cells.

4. The apparatus of claim 1, wherein the first and second memory cells are static RAM memory cells.

5. The apparatus of claim 1, wherein the comparator circuit is comprised of a single comparator with a first input coupled to the first bit line and a second input coupled to the second bit line.

6. The apparatus of claim 5, wherein the output of the comparator is coupled to a latch to store an indication that the voltage level on the first bit line differs substantially from the voltage level on the second bit line.

7. The apparatus of claim 6, wherein the time at which the latch is triggered is adjustable.

8. The apparatus of claim 6, wherein the latch is a sticky latch that is triggered to latch an indication that the voltage level on the first bit line differs substantially from the voltage level on the second bit line at any time that such an indication takes place.

9. The apparatus of claim 1, wherein the comparator circuit is comprised of:

a subtracting circuit with a first input coupled to the first bit line and a second input coupled to the second bit line;

a first comparator coupled to the output of the subtracting circuit; and

a second comparator coupled to the output of the subtracting circuit.

10. The apparatus of claim 9, wherein:

the output of the first comparator is coupled to a first latch to store an indication that difference in voltage levels between the first bit line and the second bit line has risen above a first reference voltage; and

the output of the second comparator is coupled to a second latch to store an indication that the difference in voltage levels between the first bit line and the second bit line has dropped below a second reference voltage.

11. The apparatus of claim 10, wherein the first and second reference voltages are adjustable.

12. The apparatus of claim 10, wherein the time at which the first and second latches are triggered is adjustable.

13. The apparatus of claim 10, wherein the first and second latches are sticky latches such that the first latch will latch any indication that the differences in voltage level between the first and second bit lines has risen above the first voltage reference and the second latch will latch any indication that the differences in voltage level between the first and second bit lines has dropped below the second reference voltage.

14. A method, comprising:

writing identical values to the first and second memory cells;

coupling a first memory cell to a first bit line;

coupling a second memory cell to a second bit line;

coupling the first and second bit lines to inputs of a comparator circuit;

reading the identical values from the first memory cell through the first bit line and from the second memory cell through the second bit line;

comparing the voltage levels on the first and second bit lines.

15. The method of claim 14, further comprising latching an indication from the comparator circuit that the voltage level of the first bit line differs substantially from the voltage level of the second bit line.

16. The method of claim 14, further comprising setting the degree to which the difference in voltage levels between the first bit line and the second bit line is substantial.

17. A comparator circuit in a memory array comprising:

a first input coupled to a first bit line that is coupled to a first memory cell in the memory array;

a second input coupled to a second bit line that is coupled to a second memory cell in the memory array; and

an output coupled to a sticky latch.

18. The comparator circuit of claim 17, wherein the comparator circuit is coupled to a multiplexer to disconnect the second bit line, and to connect a third bit line that is coupled the first memory cell in the memory array.